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Scalable Platform for Nanocrystal-Based Quantum Electronics

Joachim E. Sestoft,* Aske N. Gejl, Thomas Kanne, Rasmus D. Schlosser, Daniel Ross, Daniel Kjær, Kasper Grove-Rasmussen, and Jesper Nygård*

Unlocking the full potential of nanocrystals in electronic devices requires scalable and deterministic manufacturing techniques. A platform offering compelling paths to scalable production is microtomy, the technique of cutting thin lamellas with large areas containing embedded nanostructures. So far, this platform has not been used for the fabrication of electronic quantum devices. Here, microtomy is combined with vapor–liquid–solid growth of III/V nanowires to create a scalable platform that can deterministically transfer large arrays of single and fused nanocrystals—offering single unit control and free choice of the target substrate. Electronic devices are fabricated on cross-sectioned InAs nanowires with good yield, and their ability to exhibit quantum phenomena such as conductance quantization, single-electron charging, and wave interference are demonstrated. Finally, it is devised how the platform can host rationally designed semiconductor/superconductor networks relevant to emerging quantum technologies.

1. Introduction

Processing of nanocrystals (NCs) in scalable and deterministic ways is critical for their use in research fields ranging from new types of transistors[1–3] to biosensors,[24,5] optoelectronics,[2–6,8] and modern quantum devices.[9–11]

Generally, there are two approaches to scalable processing of NCs. One route is substrate dependent; here the NCs are either grown or etched from specific substrates, which also support later fabrication steps (e.g. circuit manufacturing). The second method is predominantly transfer-based; here the NCs are first synthesized and then later transferred to a specialized substrate. The techniques favored for the substrate specific approaches are vapor–liquid–solid growth (VLS), metalorganic vapor-phase epitaxy, selective area epitaxy, Stranski–Krastanov growth, anisotropic etching, or flame transport synthesis.[12–15] These techniques achieve excellent crystal quality and good control of position, but since devices are fabricated on the growth substrates, device performance can suffer from substrate-induced strain, substrate/NC dislocations, short-circuiting, or sub-optimal conditions for heterostructure growth. Promising transfer-based approaches are Langmuir–Blodgett deposition,[16,17] nanocombed deposition,[18] dry transfer printing,[19] and capillary force assembly[20] which allow for high precision placement and good yield. However, they are often solution-based and depend on preparation of the target substrates which influences device architectures and inhibits tracking of individual units.

An alternative route seeking to combine the best of both approaches is nanoskiving—the technique of embedding materials in a resin and cutting extremely thin samples by an ultramicrotome. Prior works have yielded several attractive and scalable nanostructures for use in optical and electrical applications.[21,22] As an example, the fabrication of complex optically active nanostructures covering areas of several mm² has been demonstrated.[23] and also, nanoskiving was combined with etching of core–shell nanowires to form AlGaAs nanocylinders with tunable dimensions for optical devices.[24] Nevertheless, nanostructures produced by nanoskiving have not been implemented into quantum electronics.

In this work, we present a flexible platform for transferring and positioning of arrays of high quality NCs and NC networks to almost any substrate - achieved by combining microtomy with VLS growth of III/V nanowires. We measure electronic NC devices operated as field effect transistors (FETs) and find excellent mobilities as expected for InAs-based transistors, as well as quantum transport signatures when devices are operated at cryogenic temperatures. We show how the platform can be extended to host complex networks and semiconductor/superconductor devices with the prospect to realize many new types of gate-tunable superconducting qubits.[9,10,25,26] In addition, our invention may allow for alternative routes in research fields such as deterministic placement of quantum dots for realization of the Hubbard model.[27,28]
logic controlled by electrical fields[29] and single photon sources based on III/V quantum dots.[30]

2. Scalable Nanocrystal Platform

In Figure 1 we show the principles of the scalable NC device platform. InAs nanowires are grown on (111)B InAs substrates by the VLS process where the position of the nanowires are controlled by placing Au catalyst particles via electron beam lithography (EBL). Following growth the substrate is cleaved into pieces that are compatible with the microtome setup and embedded in a resin. The resin block containing the positioned nanowires is detached from the growth substrate and is mounted and aligned in the microtome setup. This work flow is illustrated in Figure 1a. Using the microtome setup we cut thin (~70–100 nm) slices of resin (lamellas), containing positioned NCs as seen schematically in Figure 1b. We find that the NCs typically extend ~60 nm out from the lamella. The lamellas can be transferred to almost any type of substrate via the liquid medium in the trough (knifeboat). Figure 1c shows a bright-field (BF) transmission electron microscope (TEM) image of an array of NCs whose relative location is translated from the growth substrate to the TEM grid. A close-up TEM micrograph of an individual NC with a clear hexagonal morphology is seen in Figure 1d. The inset shows the selected area electron diffraction (SAED) pattern where the regularly spaced spots indicate that the crystal remains intact after the sectioning/transfer process, and the gray rings correspond to the amorphous carbon grid. Additional information on the use of a ultramicrotome to create lamellas with arrays of NCs can be found in the Section S1, Supporting Information.

Following the initial transfer to a TEM grid, we transfer the subsequently cut lamella to a Si++/SiO₂ substrate. The NCs in the lamella are contacted electrically using standard cleanroom fabrication techniques as seen schematically in Figure 1e, where an array of four NCs are contacted. Details
on fabrication can be found in the Section 7. The NCs sit in plane with the lamella and the Ti/Au contacts are placed on top of the resin, resulting in the NCs being electrically accessed from the top cut facet. Since the resin is insulating the NCs are electrically isolated from each other and one can apply a voltage bias, $V_{SD}$, across the individual NCs and measure the current, $I$. The inset in Figure 1e shows a false-colored scanning electron microscope (SEM) image of one of the measured devices. In Figure 1f we show a histogram of the two-probe resistances of 15 working devices out of 17 measured at room temperature. The resistances are mostly similar in the few kΩ-regimes showing that ohmic contacts can be reproducibly fabricated. Further analysis of the cut face quality and compression effects can be found in Section S2, Supporting Information.

Concluding on this section, we expect the scalable NC platform to be easily extended to a large number of materials relevant for fabrication of quantum devices. Materials such as Si, GaAs, BiTe, Al, AlO₂, Cu, and Au have already been investigated by commercial ultramicrotome manufacturers,[31] and highly relevant materials such as Al, Pb, Sn, As, In, Ga, Ge, Sb, Bi, SiO₂ among many others are either proven or predicted to be intact after microtoming.[22]

3. Nanocrystal FETs

Having demonstrated the scalable device platform we explore the field effect behavior in a series of individual and merged InAs NCs. In Figure 2a we show a cross-section schematic of a single NC FET device with an inset showing a false-colored SEM image of one of the measured devices. At cryogenic temperatures nine of the 15 devices were still conducting and exhibited a field effect response. In Figure 2b we show the TEM images of the NCs corresponding to the device-NCs of which transport data is presented. As an example, we show the SEM image of a device fabricated on a NC (ID7) and a TEM image of a NC from the same nanowire. We investigate both NCs sectioned from single nanowires (ID6, 7, 13, 15, 17, 18), as well as devices that were fabricated on two or more merged NCs (ID2, 8, 10). One NC (ID6) is not shown due to unfortunate lamella placement on the TEM grid. The merged NCs were cut from nanowires that were deterministically grown together during a radial growth step as described in the final section. Details can be found in Section 7 and recently published work.[32] The hexagonal shapes of the single NCs appear somewhat irregular, which is an artifact from the close spacing of the single nanowires grown under unoptimized conditions. As inter-nanowire
spacings decrease local growth parameters change due to temperature fluctuations and variations in shared collection areas.

In Figure 2c we show current measured as a function of backgate voltage, $V_{BG}$, at different bias voltages, $V_{SD}$, of a NC device (ID6) at low temperature, $T = 40$ K. We choose this temperature since most conductance resonances are averaged out by thermal effects as shown in Section S3, Supporting Information. By sweeping $V_{BG}$ we modulate the number of carriers in the semiconductor and change the current flowing across the NC, bringing the device through three distinct regions. In the range $V_{BG} = 0$–2 V no current is running corresponding to an OFF state. From $V_{BG} = 2$–4 V the current increases linearly, while the current saturates above $V_{BG} = 4$ V. The saturation current increases linearly with $V_{SD}$ implying that high quality ohmic contacts to the NCs have been fabricated, as expected from n-type InAs-based electronic devices.\[39\]

We now shift our focus toward the mobility of the NCs. The FET mobility is estimated using a commonly used expression for nanowire FETs.\[34\] Details on fitting are found in Section S5, Supporting Information. We apply this model to underline the overall FET behavior of NC devices. Figure 2d shows the linear conductance measured (G) as function of $V_{BG}$ where the corresponding fit follows the behavior of the FET excellently until close to pinch-off. The inset shows a zoom-in on the subthreshold swing, SS, of the $I/V_{BG}$ curve at $V_{SD} = 175$ mV from Figure 2c. Depending on the chosen range, the SS varies between $\approx 0.5$–1 $V$ dec$^{-1}$ which is significantly lower than state-of-the-art nanowire FETs.\[35,36\] This behavior may be explained by the extremely short distance between the contacts resulting in short channel effects which are known to reduce the SS in ultra short devices.\[37\] Additional hysteresis plots are shown in Section S4, Supporting Information, and are comparable to other types of nanowire-based FETs fabricated on Si$^{17}$/SiO$_2$ substrates.\[34\]

We have estimated the low temperature mobilities for all nine NC FETs as seen in Figure 2e ($T = 2.8$ K). Output measurements and linear conductance traces with according fits are shown in Section S5, Supporting Information. We observe no noticeable trend between the estimated mobilities obtained from NCs cut from a single nanowire or merged nanowires indicative of no significant barrier in the merged NCs. This may be explained by specific growth conditions causing the merged NCs to effectively act as a single crystal, hence suggesting that formation of larger networks based on current growth parameters is feasible. The estimated mobilities seem comparable to or larger than values found in SAG and VLS grown InAs and InSb nanowires\[34,38\] although they vary across the different devices. These variations may be attributed to variations in gate capacitance and small device dimensions. For one, large variances in effective gate-capacitance may produce different mobility estimations. In addition, the model accounts for diffusive transport whereas some device lengths are comparable to or smaller than the mean free path of InAs nanowires ($\approx 150$ nm).\[38\] Hence, we use the FET model mainly to highlight the predictable field effect behavior of the NC devices. We note that any unevenness in the hexagonal shape of some of the single NCs seen in Figure 2b, stems from down-stream effects of nanowires grown in close proximity. As the inter-nanowire spacing is smaller than the mean diffusion length of the growth material the substrate adatom population will be uneven, resulting in adjacent nanowires having different adatom contributions and hence varied effective flux ratios. In particular, this can influence the growth dynamics in the axial nanowire growth phase resulting in local diameter variations. In summary, this section shows that the NC transfer platform can host ultra-small FET devices and that these behave predictably in electrostatic fields, which is a fundamental requirement for control of complex electronic quantum devices.

4. Quantum Transport in Single Nanocrystals

A prerequisite for using the NC platform for quantum-based applications is the capability to hold quantized phenomena in single NCs. Here we show a series of quantum effects that emerge around liquid He temperatures in a set of devices based on single NCs.

We plot differential conductance, $g = dI/dV_{SD}$, as function of $V_{SD}$ and $V_{BG}$ in a waterfall plot for device ID7 as seen in Figure 3a. As we sweep $V_{BG}$ and $V_{SD}$ we observe a bunching of the individual traces close to the first few units of twice the conductance quantum ($2G_0 = 2e^2/h$) around zero bias. At larger bias voltages ($|V_{SD}| \approx 3–4$ mV) this bunching effect is no longer observed at integer values but instead at half-integer values. These effects are discussed based on the inset shown in Figure 3a where a schematic of the parabolic dispersion relation of the first few sub-bands in an ideal 1D quantum point contact (QPC) is seen. This textbook example assumes that the device length is much smaller than the mean free path ($L_{\mu} \approx \lambda_0$), that the temperature of the system is smaller than the subband spacing ($k_B T < E_2 - E_1$) and that the Fermi wavelength is comparable to the width of the constriction ($\lambda_F \approx W$). Changing the Fermi level in the case with zero bias ($\mu_L = \mu_R$) will modulate the energetically accessible modes supported by the QPC in an integer fashion where right and left moving carriers are kept in equilibrium thus increasing conductance in steps of $2G_0$. Conversely, by applying an offset in the bias ($\mu_L \neq \mu_R$) another mode can now be accessed exclusively by for example, left moving carriers resulting in an increase in conductance by only one $G_0$.

We find that the distance between the contacts (determined by SEM to $W < 100$ nm) is smaller than the experimentally determined mean free path in InAs nanowires ($L_{\mu} = 150$ nm$^{33}$) and that the thermal energy of the system ($k_B T = 0.06$ meV) is much smaller than the estimated zero-field sub-band spacing ($E_2 - E_1$) of $\approx 3$–5 meV. However, as the width of the NC-device is larger than the Fermi wavelength typically found in InAs nanowires ($\lambda_\text{InAs} = 20–30$ nm$^{38}$), the system is likely only quasi 1D. We note that as we sweep $V_{BG}$ the confinement potential of the electron path through the device may be changed. Hence by operating $V_{BG}$ at negative voltages and taking into account screening from the leads a saddle-shaped confinement potential with a width that is comparable to $\lambda_F^{InAs}$ may be formed in the device. This behavior and the quality of data is comparable to measurements on quantum point contact-like devices based on InAs nanowires.$^{39,40,43}$ A total of three devices show zero-bias traces with according behavior as seen in Section S6, Supporting Information.
When operating at larger negative $V_{BG}$ the device is brought into the tunneling regime, likely due to opposing fields from the contacts acting as barriers for low carrier densities.\[^{[44]}\] In Figure 3b we show a color plot of $g$ versus $V_{SD}$ and $V_{BG}$ obtained from device ID7 at $T = 2.9$ K. Here we observe diamond shaped conductance resonances with the dark blue regions inside the diamonds corresponding to transport being suppressed by Coulomb blockade. In the inset in Figure 3b we show an illustration of an energy diagram for a quantum dot (QD) tunnel-coupled to a source and a drain contact. When the chemical potential is modulated in the zero-bias case ($\mu_1 = \mu_R$, not shown in illustration) single quantum mechanical states in the QD are accessed as the charging energy ($E_C$) determined by the electrostatic force of the system is overcome. Applying a bias offset ($\mu_L \neq \mu_R$) to this model allows us to measure the addition energy ($E_{add}$) as the source and drain potentials are aligned with the energy of the quantum state where the conductance resonances are observed. From the shape of the diamonds we extract the charging energy, $E_C = 75$ meV, total capacitance, $C_{tot} = 22$ aF, gate capacitance, $C_g = 0.9$ aF, and lever arm $\alpha = 0.03$. The quantum confinement energy is tentatively estimated to $\Delta = 12.5$ meV. These findings are similar to values found in literature for a variety of self-assembled and nanowire-based InAs quantum dots.\[^{[41,44–47]}\] Quantum dot-like structures were also observed in device ID 6. Additional data on excited states are shown in Section S7, Supporting Information.

In Figure 3c we show conductance spectroscopy of device ID6 where a checker-board pattern on a background of conductance is seen. When electronic waves are backscattered from a set of opaque barriers (as seen in the inset in Figure 3c), likely residing at the NC/contact interface, resonant conductance features may appear as either the chemical potential or the potential landscape of the device is changed. This is analogous to the transmission/reflection of light waves in Fabry–Pérot cavities. By converting $C_F$ extracted from Figure 3b into capacitance per unit length ($C_F = 6$ pF m$^{-1}$), and taking the spacing between the oscillations at zero bias, $\Delta V_{BG} = 250$ mV, we can estimate the length of the Fabry–Pérot system to be $L = \frac{2e}{C_F \Delta V_{BG}} = 215$ nm, which is comparable to the width of the NC measured by SEM. As we sweep $V_{BG}$ the finite conductance background is modulated and a large variation in $\Delta V_{BG}^{FP}$ is observed suggesting that the number of Fabry–Pérot modes present in the NC device changes. Similar behavior was observed in device ID2. These findings are comparable to electronic Fabry–Pérot interference found in nanowires and nanotubes.

Concluding on Figure 3, we demonstrate the ability of the NC devices to hold three fundamental types of electronic quantum phenomena.

5. Networks and Hybrid Devices

Recently, controlled growth of merged superstructures of nanowires has been demonstrated,\[^{[32]}\] as well as semiconductor/superconductor nanowire heterostructures composed of III/V materials and Sn, Pb, and Al, known as hybrid devices.\[^{[52–58]}\] These emerging materials are in high demand as they are proposed to serve as a foundation for emerging quantum information technologies.\[^{[9–11]}\] Here we show how to extend the presented NC platform to these new material combinations and complex device architectures.

In Figure 4a, a schematic of a growth substrate is presented where the dashed lines indicate a coordinate system. By use of standard EBL processes, catalyst particles can be placed on the growth substrate in predetermined patterns, and when VLS growth is initiated nanowires are formed at the locations of the catalyst particles.\[^{[32]}\] Given the conditions under standard VLS growth (see Section 7 for details) the nanowires grow predominantly in the vertical direction with respect to the InAs (111)B substrate, and only minimally in their radial directions ($\{110\}$). Controlling the design of the catalyst particle placement, this can result in extremely closely spaced single nanowires, as illustrated in the cross-section view in Figure 4a(i). From arrays of individual nanowires, one can merge nanowires along their growth directions in order to form networks (see Figure 4a(ii) for cross-section schematic) in two ways.
With the first approach, single nanowires are grown with a small separation (≈50 – 160 nm) from large volume seed particles. As the seed particle volume determines the width of the nanowires, this ensures that the nanowires are rigid. After reinitiating growth in a second growth step (see Section 7) the nanowires grow predominantly in the radial directions. Depending on the placement of the single nanowires, we can merge two or more nanowires into networks, and control the extent of which they merge. In Figure 4a(ii),b, we show a cross-section schematic and an SEM image of an example of three nanowires merged during radial overgrowth, respectively.

With the second approach, nanowires are also grown with a small separation but from smaller volume seed particles, such that the resulting nanowires are thin. Local vibrations and van der Waals forces then make the nanowires touch and stick during the first growth phase, and allow the small amount of radial growth still present during the VLS mechanism to merge the individual nanowires. We provide examples of this in the SEM and cross-section TEM image shown in Figure 4c,d.

After growth, these structures are embedded and sectioned as already described, creating networks of connected or disconnected semiconductor islands. Additionally, they can be grown with a superconductor (Al) as seen in the illustration in Figure 4a(iii) and the TEM image in Figure 4f.

Based on the first scheme, we have designed and grown complex nanowire network structures as seen in Figure 4d,e. We highlight these particular structures as combinations of these after sectioning can form myriads of complex NC-based device structures, simply by controlling the placement of the seed particles. The erratic growth on the nanowire ends can be alleviated by optimization of growth parameters. In Figure 4g, we showcase how the presented platform can be used to assemble a type of device (superconducting hybrid island) that has obtained widespread attention lately for research into Majorana physics in semiconductor/superconductor nanostructures.[9–11]

6. Conclusion and Outlook

We combine two well-established techniques—growth of nanowires and microtome—to make a scalable platform for production of electronic quantum devices. The platform is generic in that it is not limited to VLS grown nanowires, but can be extended to other growth or etching-based techniques allowing the platform to use a broad range of materials. Based on the placement of catalyst particles and controlled crystal overgrowth, we show how this platform can be extended to NC networks of unprecedented shapes and be merged with semiconductor/superconductor technologies to build complex
superconducting quantum devices. We expect the NC-transfer platform to be ideal for realizing large arrays of quantum dots with specifically tailored tunneling barriers. This is an interesting new route for quantum information technology and fundamental studies, such as development of lattice-based quantum simulators and wireless single-electron logic controlled by AC-fields.[27,29]

During device fabrication, selected lamellas can be used as samples for quality control for example, AFM, TEM, and SEM, which is expected to become a desirable feature when transitioning technologies from prototype to high-throughput manufacturing.

Future work should investigate alignment optimization between the nanowire high symmetry crystal axes and the microtome knife cut plane to improve crystal cleaving and NC morphologies. In addition, different routes for improving transport signatures should be explored such as atomic layer deposition of high-x dielectric materials prior to microtoming, removal/change of the resin, and in situ deposited contacts. Additional routes not investigated here involve growth of radial heterostructure p–n NCs embedded in a transparent resin for production of optoelectronic devices. Additionally, stacking of multiple lamellas containing NCs with deliberately tuned p–n junctions could be used for high efficiency tandem solar cells. This principle could be further extended for extreme downscaling inter-pixel pitch between RGB sub-units for ultra high resolution monitors.

In conclusion, this platform provides a new approach to nanoscale device engineering with prospects for scalable fabrication and opens up new ways to integrate nanomaterials into emerging technologies within the fields of optics, optoelectronics, electronics, and quantum devices.

7. Experimental Section

**Nanowire Growth:** A molecular beam epitaxy (MBE) system was used to grow Au-seeded wurtzite InAs nanowires along the [0001]B direction on InAs (111)B substrates using the VLS mechanism. Arrays of Au catalyst particles were placed via standard EBL with particle radius \( r_{\text{Au}} = 20–120 \text{ nm} \) and height \( h_{\text{Au}} = 10–50 \text{ nm} \). The native oxide was removed by annealing the growth substrate at \( T = 500 \text{ C} \) for 5 min under As overpressure before predominantly vertical nanowire growth was initiated at growth temperatures ranging from \( T_{\text{growth}} = 445–450 \text{ C} \). Axial nanowire growth was carried out for a duration of 10–120 min before a short break (5 min) was introduced and the \( \text{As}_2/\text{As}_4 \) ratio was increased.

After vertical nanowire growth was concluded, growth conditions favoring radial growth were established. First, a short pause (5 min) was introduced before the temperature of the growth substrate was lowered steadily to \( T_{\text{growth}} = 350 \text{ C} \) over about 15 min. After an additional pause (5 min) the nanowires were radially overgrown for 1–20 min depending on the desired amount of overgrowth and distance between Au particles. An exhaustive description can be found in recently published work.[32]

**Microtomy:** InAs growth substrates were cleaved into smaller pieces containing the as-grown nanowire arrays. The wafer pieces were placed into silicone molds with the growth substrate facing the bottom, such that the nanowires were orientated toward the mold opening. Next, the embedding solution was prepared using the SPURR Low-Viscosity resin applying the “hard” epoxy recipe. Ten samples were created from mixing 4.10 g ERL 4221 (cyloaliphatic epoxide resin), 0.95 g diglycidyl ether of polypropylene glycol, 5.90 g nonenyl succinic anhydride, and 0.10 g dimethylaminomethanol. The mold was then filled with the solution before it was baked for 8 h at 70 °C to harden the resin. Now the growth substrate was removed from the sample using a razor blade leaving the nanowires embedded, before the block-face dimension was trimmed to accommodate our device blanks (≈250 × 250 μm). The trimmed samples were mounted in a Leica Ultracut UC7 Microtome and sectioned with a DiATOME Ultra 45° diamond knife at a clearance angle of 6°. After sectioning the lamellas were floating on top of the fluid (ultra-pure water) contained by the knife boat. The desired substrate was partially submersed, the lamellas were guided to the desired location and the substrate withdrawn now containing the deposited lamellas. In this case lamellas were transferred to Si++/SiO_2 substrates, glass slides, and TEM grids.

**Microscopy:** TEM characterization of the NCs in the lamellas was performed using a 200 kV Philips-Fei CM20 large tilt TEM. The plane waves were aligned parallel to the [0001] zone axis of the NCs. High-resolution TEM images were obtained using a Jeol 300F microscope. SEM characterization of the substrates with as-grown nanowires were carried out with a Jeol 7800F SEM using acceleration voltages in the range of \( V_{\text{acc}} = 1–20 \text{ kV} \). A Raith Eline system was used to obtain TEM images of the deposited lamellas containing NCs and finished devices using acceleration voltage, \( V_{\text{acc}} = 10 \text{ kV} \). The cut-face quality of the NCs post-sectioning was inspected by AFM using a Bruker Dimension Icon PT AFM in PeakForce Tapping mode.

**Device Fabrication and Measurement:** All devices were fabricated on highly doped Si++ substrates covered by 200 nm of thermal oxide. Prior to device fabrication SEM was used to verify the position of the NC and that the morphology remained intact after microtoming. Metallic leads to the NCs were fabricated by electron beam lithography. RF ion (Ar+) milling was performed in the metal deposition chamber prior to e-beam metal deposition of Ti and Au (5/200 nm) to create transparent ohmic contacts to the NCs. Standard low-frequency (<200 Hz) lock-in measurements were performed to measure differential conductance \( (V_{\text{acc}} = 5–20 \mu \text{V}) \). No data correction was performed on the electrical data.

**Supporting Information**

Supporting Information is available from the Wiley Online Library or from the author.

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**Conflict of Interest**

The authors declare no conflict of interest.

**Author Contributions**

the microtomy. J.E.S. and A.N.G. fabricated devices. J.E.S., A.N.G., and R.D.S. carried out the transport measurements. T.K., J.E.S., and J.N. developed the materials. J.N. supervised the project. All authors contributed to analyzing and interpreting the data and to writing the manuscript.

Data Availability Statement
All raw data and curated data sets are provided online at https://erda.ku.dk/archives/335ba013276d360019209d7b80fba323/published-archive.html.

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