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Shadow epitaxy for *in-situ* growth of generic semiconductor/superconductor hybrids

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Uniform, defect-free crystal interfaces and surfaces are crucial ingredients for realizing high-performance nanoscale devices. A pertinent example is that advances in gate-tunable and topological superconductivity using semiconductor/superconductor electronic devices are currently built on the hard proximity-induced superconducting gap obtained from epitaxial indium arsenide/aluminium heterostructures. Fabrication of devices requires selective etch processes; these exist only for InAs/Al hybrids, precluding the use of other, potentially superior material combinations. We present a crystal growth platform – based on three-dimensional structuring of growth substrates – which enables synthesis of semiconductor nanowire hybrids with *in-situ* patterned superconductor shells. This platform eliminates the need for etching, thereby enabling full freedom in choice of hybrid constituents. We realise and characterise all the most frequently used architectures in superconducting hybrid devices, finding increased yield and electrostatic stability compared to etched devices, along with evidence of ballistic superconductivity. In addition to aluminium, we present hybrid devices based on tantalum, niobium and vanadium.

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One-dimensional semiconductor (SE) nanowires (NWs) proximity coupled to superconductors (SU) have attracted considerable attention from the condensed matter community since the prediction and observation of Majorana zero-modes, which have been proposed as a basis for topologically protected quantum information processors.

To ensure topological protection, methods for growing disorder-free ‘hard-gap’ SE/SU epitaxial hybrids were developed. These materials use bottom-up crystal growth of InAs NWs with uniform epitaxial aluminium coatings, an approach which has been extended to high mobility two-dimensional systems and selective area grown networks.

The success of epitaxial InAs/Al hybrids lies in the ability to selectively remove the Al via top-down processing, and thereby realise important device classes such as normal metal spectroscopic devices and Josephson Junctions for gate-controlled transmon qubits and superconducting Majorana islands.

A limitation of this method is that the need for post-process etching inherently limits materials choice. For instance, despite strong incentives to utilise technologically important superconductors such as Nb and NbTi, which exhibit higher transition temperatures, critical magnetic fields and superconducting energy gaps – selectively removing Nb from InAs remains an unsolved problem. Similarly, while InSb is an attractive semiconductor due to its high mobility, g-factor and strong spin-orbit coupling, there is no reported method for selectively removing even Al from InSb without damage. Thus, most potential improvements in epitaxial SE/SU technology are predicated on developing a materials-independent method for device fabrication. An attractive approach to eliminating etch processes is to employ an *in-situ* ‘shadow approach’ that masks specific segments along the NW from superconductor growth. Initial progress was demonstrated in Refs. where deterministically positioned NWs were shadowed by adjacent NWs. This approach, however, requires accurate control of relative NW positions and growth directions. Further, the range of the possible device geometries is limited, since the NWs create only narrow gaps in the SU coating.

Here, we demonstrate a flexible platform for growing device-ready hybrids in numerous geometries. We combine pre-growth fabrication of shadow structures directly on NW growth substrates with precise positioning of NW growth sites and full *in-situ* control of the orientation of superconductor flux. The shadow epitaxy platform enables independent materials choice (SU,SE) and we demonstrate simultaneous growth of the most important hybrid device architectures using aluminium, niobium, tantalum and vanadium.

Eliminating post-process chemical etching increased spectroscopic device yield (5 out of 5 for Al and Ta devices), enabled ballistic superconductivity in Nb devices, and enhanced electrostatic stability by an order of magnitude in Majorana island devices. Very high yield and large-range, hysteresis-free device operation are crucial metrics for future advanced circuitry that incorporates a large number of hybrid devices.
FIG. 1. Shadow epitaxy platform for hybrid nanowire growth. a, False colour scanning electron micrograph (SEM) of SiOx (blue) bridges spanning trenches in an InAs (grey) substrate. InAs nanowires (NW) are grown in proximity to the bridges, which act as a shadow mask. Inset: Overview SEM of bridge substrate before growth. b,c, Schematics viewed from b, side and c, the direction of superconductor (yellow) deposition. Direction of superconductor deposition is shown by the arrows in b. The bridge geometry is projected onto each NW to lithographically define the regions left uncoated during superconductor deposition. d-h. False colour SEMs of as-grown NW hybrids with Al overlayer (yellow) with d, half-shadowed/tunnel spectroscopy, e, Josephson junction, f, island and g, double island geometries. S and N indicate the superconducting and bare NW segments, respectively. Scale bars represent a, 5 µm (main) and 50 µm (inset) d-g, 2 µm (left images) and 500 nm (right images).

THE SHADOW EPITAXY PLATFORM

Figure 1 illustrates the platform features. A (111)B-oriented InAs growth substrate is patterned with etched trenches and a series of silicon oxide (SiOx) ‘bridges’. NWs are grown from gold catalyst particles, pre-positioned at the trench bottom with the desired lateral distance from the overhanging bridge(s). NWs are grown by molecular beam epitaxy and the bridges act as shadow masks for subsequent in-situ deposition of superconductors, normal metals, or dielectrics. The material is deposited from a direction parallel to the trenches and inclined by an angle $\theta = 5 - 45^\circ$ from the substrate surface.
growth and superconductor deposition. In the simplest, single-deposition case, the superconductor coats 2 or 3 of the NW’s 6 facets – i.e. a half-shell coating – except for regions shadowed by the bridge. This breaks the NW into a sequence of SU segments separated by bare SE. The length and number of segments are controlled by $\theta$ and the projected bridge design (Supplementary Section 2). Additional possibilities using multiple depositions, angles and/or materials are demonstrated below (Figure 5). Figure 1e-g show scanning electron micrographs (SEMs) of bridges designed to produce the four most important hybrid device geometries. Half-shadowed NWs (Figure 1d) are the canonical design for tunnel-spectroscopy characterisation of the (sub)gap properties of hybrids and are obtained by shadowing the entire lower section of the NW with a wide bridge. A single, narrow bridge (Figure 1e) produces a gate-tunable Josephson junction, the component at the heart of gatemon and Andreev qubits. Double and triple bridges (Figure 1f,g) produce hybrids with single and double Majorana island geometries, respectively, which are the building blocks of topological quantum computation schemes. In summary, the shadow epitaxy platform enables materials-independent, wafer-scale, parallel synthesis of device-ready hybrids, in many different geometries.

**PATTERNING AND STRUCTURAL CHARACTERISATION OF SU FILMS**

The SU and SE feature sizes are largely defined by the shadow epitaxy mask used, although evaporation chamber geometry and material diffusion become important when high precision is required. In particular, the finite evaporation source size and the distances between NW, mask and source generate ‘tail regions’ between fully covered and fully shadowed segments (Supplementary Section 2). The expected tail length is $l_t = 100 - 200$ nm for our mask/chamber dimensions. To characterise this, Figure 2 shows SEM and transmission electron micrographs (TEMs) of InAs hybrids with Al, Ta and Nb shells. Depositions were performed using e-beam evaporation at room temperature except for Al, where $T \sim -150^\circ$C (see Methods), with thicknesses $t_{Al} = 8$ nm, $t_{Nb} = 40$ nm, $t_{Ta} = 20$ nm (left and middle panel) and $t_{Ta} = 5$ nm (right panel). Figure 2 middle panels show typical $l_t = 65 - 120$ nm for Nb/Ta and $l_t < 60$ nm for Al. The smaller-than-estimated $l_t$ suggests that material diffusion acts to shorten $l_t$. The enhanced diffusion and associated shorter $l_t$ for Al is expected from the lower heat of vapourisation $\Delta H_{vap}^{Al} \sim 300$ kJ/mol, c.f. $\Delta H_{vap}^{Ta,Nb} \sim 700$ kJ/mol. Note that these effects can be compensated for by, e.g., altering mask design and NW position, using a smaller deposition source or collimator, and/or double-angle evaporation (Supplementary Section 2).

The semiconductor/superconductor interface proper-

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**FIG. 2.** SEM (left panels) and TEM (middle and rightmost panels) of half-shadowed, half-shell hybrid materials grown using the shadow epitaxy platform. a. Al/InAs shadow hybrid with 8 nm thick Al deposited at $T = -150^\circ$C, exhibiting an epitaxially matched interface. b. Tantalum (middle panel 20 nm thick; right panel 5 nm thick) and c. niobium (40 nm thick) films exhibited nanocrystalline/amorphous structure. The length $l_t$ of the tail at the SU shadow edge was determined by the geometry of the mask and chamber, as well as material diffusion (Supplementary Section 2). Ta and Nb had typical $l_t \sim 65 - 120$ nm and Al $l_t \leq 60$ nm. The broad bright/dark fringes in low-resolution TEM (middle panels) are likely bending contours, whereby slight bends in the NW result in modulation of the crystal plane orientation with respect to the beam. Scale bars represent 500 nm (left images), 100 nm (middle images) and 1 nm (right images).

The situation is schematically shown in Figure 1b,c. The bridge design is thereby projected as a pattern in the superconducting layer on each NW, effectively growing the desired device architecture, with independent choice of SE and SU material. For process details see Methods and Supplementary Section 1.

To ensure a pristine interface, the sample remains under ultra-high vacuum ($< 10^{-8}$ Torr) between NW...
FIG. 3. Induced superconductivity in Al/InAs, Ta/InAs and Nb/InAs hybrids. a, False-color SEM of InAs NW (grey) with shadow patterned Al (purple) and ex-situ Ti/Au contacts (gold). Scale bar represents 500 nm. b, Differential conductance $G = dI/dV_{sd}$ vs. $V_{sd}$ and $V_g$ close to pinch-off. A continuous, hard gap with $\Delta = 0.25$ meV and sub-gap states are evident. c, Measured $G$ vs. $B_\perp$ for $V_g$ fixed at the position of the line trace in b shows the gap closing at $B_\perp \sim 2$ T. A peak at zero bias emerges at $B_z = 1.3$ T from coalescing bound states $d$, Typical measurements of $G$ (normalised to $G_N$ at $V_{sd} = -0.4$ mV) vs. $V_{sd}$ on a logarithmic scale. A hard superconducting gap is found for all five Al/InAs devices, A1-A5. e, Corresponding measurement for Ta/InAs devices ($G_N = G(V_{sd} = -0.25$ mV)). Traces in d,e are offset by two decades for clarity. f, $G$ vs. $V_g$ for a Nb/InAs device exhibiting conductance plateaus for $V_{sd} = 0.5$ mV $> \Delta$ at multiples of $0.7 \times 2e^2/h$ (dashed lines), and conductance doubling in the superconducting state, $V_{sd} = 0$. g, $G$ vs $V_{sd}$ shows conductance doubling on the first plateau at $V_g = -10.25$ V, and a soft gap in the tunnelling regime, $V_g = -12.5, -14$ V. Contact resistance $R_C = 3.2$ k$\Omega$ was subtracted from the data in f,g.

TUNNEL SPECTROSCOPY DEVICES

Low temperature transport experiments were performed both to benchmark the shadow-patterned hybrids against the wide literature on etched epitaxial Al and Nb/InAs devices – performance gains are expected due to eliminating post-process etching. Al/InAs devices showed conductance doubling on the first plateau at $V_g = -10.25$ V, and a soft gap in the tunnelling regime, $V_g = -12.5, -14$ V. Contact resistance $R_C = 3.2$ k$\Omega$ was subtracted from the data in f,g.
tance $G(V_{sd} = -0.4 \text{ mV})$ was $\sim 75$ throughout the studied $V_g$ range, with a peak value of 350 (Supplementary Section 5). This is the highest reported figure in a SE/SU hybrid, confirming the high quality of the interface. Figure 3e shows the evolution in parallel magnetic field, $B_{\parallel}$, with $V_g$ fixed at the position of the line trace of Figure 3b. The gap closes at critical field $B_c \sim 2 \text{T}$; consistent with the thin (8 nm), flat, epitaxial film. Coalescing bound states that stick to zero energy for $B_{\parallel} > 1.3 \text{T}$ were also observed – highlighted by the line trace taken with $B_{\parallel} = 1.5 \text{T}$ – resembling previously reported topological zero modes. While a detailed analysis of zero-modes is outside the scope of this article, the magnetic field-compatibility and effective $g$-factor $= 6.5^{39}$ highlight the potential of the shadow hybrids for studying the topological regime.

In total, we fabricated five Al/InAs tunnel devices, Al1-A5, and logarithmic line traces of normalised conductance $G/G_{STAB}$ vs $V_{sd}$ at fixed $V_g$ are shown in Figure 3d. All five devices exhibited similar behaviour and a hard superconducting gap, with $G_N/G_S = 50 - 100$. Devices A2-A4 feature multiple peaks below the coherence peaks at $\Delta$ due to bound states (Supplementary Section 6). Overall, the results confirm the high quality of the Al/InAs hybrids synthesised using shadow epitaxy, and the device yield (5 out of 5) compares favourably with conventional device processing using wet etching (Supplementary Section 4).

Turning to devices grown with Ta and Nb, all five Ta/InAs devices exhibited induced superconductivity (Fig 3e). Devices T1-T4 showed hard gaps with values $G_N/G_S = 50-100$, persisting over a wide $V_g$ range (Supplementary Section 6), similar to Al/InAs hybrids. T5 showed a lower hardness $G_N/G_S \sim 10$. Since the Ta is nanocrystalline/amorphous (Figure 2b) these results show that the atomic ordering of epitaxial interfaces is not a prerequisite for hard gap superconductivity. Rather, an impurity-free, uniform interface is sufficient. The values for $\Delta_{Ta} = 0.13 \text{ meV}$ and corresponding $T^*_T = 0.7 \text{ K}$ are consistent with bulk films of matching thickness, 20 nm (Supplementary Section 7). The Ta/InAs out-of-plane critical field $B_{C1}^{Ta} \sim 3.5 \text{ T}$ (Supplementary Section 7) is significantly higher than for Al/InAs $B_{C1}^{Al} \sim 100 \text{ mT}$ with similar dimensions, making Ta/InAs hybrids potentially attractive for studies of topological superconductivity.

The technological importance of niobium based-superconductors – owing to their high $T_C \sim 9 \text{ K}$ and high critical magnetic fields – has motivated efforts to incorporate them in ex-situ-fabricated hybrid nano-devices. Shadow epitaxy enables in-situ Nb/InAs devices previously impossible due to lack of selective process techniques. Figures 3f,g present low-temperature spectroscopic results. Upon increasing $V_g$, the conductance for $V_{sd} = 0.5 \text{ mV} > \Delta$ increases in steps of $0.7 \times 2e^2/h$ and shows a doubling at the plateaus for $V_{sd} = 0$. This is consistent with a near ballistic junction and near perfect transmission at the contacts. In the tunnelling regime, $V_g \leq -12.5 \text{ V}$, conductance suppression is clearly observed for $eV_{sd} < |\Delta| \sim 0.2 \text{ meV}$ in Figure 3g, albeit with relatively low hardness ($G_N/G_S \sim 3$). Considering the near ballistic device characteristic and high contact transmission, and given the excellent gap hardness achieved in Al/InAs and Ta/InAs shadow devices, it is unlikely the soft superconducting gap for our in-situ Nb/InAs hybrid was caused by contaminated or process-damaged interfaces. Rather, native oxides at the Nb surface could provide an explanation. Nb oxides can be superconducting with lower $T_C \sim 2 \text{ K}$, metallic, or magnetic$^{43-44}$; each of these effects leads to soft-gap superconductivity in thin niobium films. Using in-situ surface passivation of Nb hybrids would likely provide insights into how the surface impacts gap properties (see Figure 5a). To summarise, the main result of Figure 3 is the demonstration of high-quality hybrid devices with expanded choice of SU and SE.

**STABILITY OF IN-SITU MAJORANA ISLAND DEVICES**

While tunnel spectroscopy devices are the essential tool for characterising induced superconductivity, the elemental building block in most topological quantum computing architectures are ‘Majorana islands’$^{11,26}$ which consist of a finite length hybrid segment retaining a charging energy $E_C$. Single$^{21}$ and double$^{22}$ island geometries with arbitrary superconductors are realised using a shadow epitaxy pattern of two or three bridges as shown in Figure 1f,g. The bridge separation(s) and widths determine the lengths of the hybrid segment(s) $\propto E_C$ and the exposed NW segments, respectively.

**Figure 4a** shows a typical Al-based shadow-patterned device, measured to enable comparison with conventional etched devices. The gate potentials $V_g$ and $V_{sd}, V_{sd2}$ control the charge on the island and the tunnel coupling to the Ti/Au leads.$^{21,23,35,36}$ For $E_C < \Delta$ and in the absence of quasi-particles or sub-gap states, charge is added in units of $2e$ (Cooper pairs). Figure 4b, shows $G$ vs. $V_{sd}$ and $V_g$ exhibits $2e$-periodic Coulomb diamonds that correspond to a charging energy $2E_C \sim 130 \text{ meV}$ (dashed lines). Quasi-particle $1e$ periodic charging is seen for $eV_{sd} > \Delta \sim 180 \text{ meV}$ (solid lines). Figure 4c shows the temperature dependence of the low-bias $V_g^*$-induced charging. The $2e$ periodic state persists up to $T \sim 250 - 300 \text{ mK}$, where a transition to $1e$ periodicity occurs due to thermal excitation of quasi-particles. This temperature is set by $\Delta$ and the volume of the superconductor and is comparable to that observed in etched devices.$^{45-46}$

A reproducible and quiet electrostatic platform is crucial for charge-based topological devices, since environmental charge fluctuations and noise couple both to the island charge and tunnel couplings through the semiconductor, and thereby constitute a direct source of qubit decoherence.$^{47-48}$ Furthermore, with increasing complex-
FIG. 4. Electron transport in a Majorana island. a, False color SEM of shadow patterned Al/InAs island device. Middle gate voltage, $V_g$, was varied, with the four other gates used to generate tunnel barriers. Scale bar represents 500 nm. b, Bias spectroscopy showing Coulomb blockade diamonds with 2e-periodicity in $V_g$ for $V_{sd} < \Delta$ and 1e-periodicity for $V_{sd} > \Delta$. c, Zero bias conductance, $G$ vs. $V_g$ and temperature, $T$. 1e-periodic peaks above $T = 250 − 300$ mK emerge due to thermally excited quasi-particles. d, A single, continuous measurement of $G$ vs. $V_g$ and $B_\parallel$, presented without corrections for, e.g., switching. 364 electrons were removed from the island. The 2e- to 1e-periodic transitions in the range $B_\parallel = 0.15 − 0.25$ T occur as bound states move to zero energy. This can occur with e, equal spacing between 1e peaks, or f, $B_\parallel$-dependant spacing, depending on the nature of the bound state. g, A parity transition to a state where only odd numbers of electrons are on the island is also possible. 

ity of topological Majorana circuits, fine-tuning in a multi-dimensional space of cross-coupled parameters is required, and stability and reproducibility become important requirements. In conventional etched devices, the stable operation range is typically limited to $< 20$ consecutive charge states as uncontrolled discrete charging of nearby impurity sites leads to random switches of the island charge/parity. The shadow device exhibits an increase of this range by at least an order of magnitude, consistent with a cleaner electrostatic environment due to the obviation of processing. This is demonstrated in Figure 4d, which shows the stable evolution of 182(364) consecutive 2e(1e) charge states accessed by continuously sweeping $V_g$, and an interleaved, step-wise increase of $B_\parallel$. The island is superconducting in this field range, and the bifurcation of the spectrum at $B_\parallel \sim 200$ mT is caused by the appearance of a bound state below the gap, as previously analysed in ad-
FIG. 5. **Advanced device geometries** a, Schematic of two-angle procedure for Josephson, or metal-NW-metal junctions protected by an *in-situ* conformal insulator coating. b, Contacting the NW with two different materials is possible using evaporation of the desired materials from different angles, $\theta_1$ and $\theta_2$. The pictured example constitutes an *in-situ* formed tunnel spectroscopy device. c, Example of vanadium Josephson junctions realised by two-angle deposition, where junction length depends on $\theta_1$, $\theta_2$ and the NW-bridge separation, $S$. d, Demonstration of a full-shell extension of the shadow concept. Depositing from six different angles matching a six-fold symmetric bridge structure aligned with the facets of the NW, yields a full-shell JJ. Scale bars represent c, 200 nm, d, 10 $\mu$m (left) and 200 nm (right).

In addition to a topological transition, various trivial effects can lead to a $2e-1e$-transition in $B_{\parallel}$, each exhibiting distinct peak spacing and amplitude modulation. Electrostatic stability is also critical here for qubit decoherence and tuning. *In-situ* JJ devices are grown using single-bridge shadows (Figure 1e), and low-temperature characterisation is presented in Supplementary Section 8, demonstrating quiet operation and gate-tunable critical currents $\sim 10$ nA, consistent with previous devices.

**ADVANCED ARCHITECTURES**

Having demonstrated the use of shadow epitaxy to realise the most important hybrid device geometries, we now discuss further extensions and the flexibility of the method. Firstly, **Figure 5a** illustrates how steep-angle depositions under rotation enable *in-situ* conformal dielectric coatings that protect sensitive interfaces, contacts, and surfaces during subsequent device processing. A second extension, illustrated in **Figure 5b**, employs consecutive shadow depositions from different angles to realise a complete in-situ junction with non-identical contact elements. Such double-angle-generated structures thus produce both lateral and axial hybrid devices incorporating, e.g., normal metal, superconducting and/or magnetic elements with pristine epitaxial interfaces. Double-angle deposition also enables JJ devices with arbitrarily short junction length, as demonstrated in Figure 5c for a vanadium based hybrid made by two depositions from different angles $\theta_1 = 16^\circ$, $\theta_2 = 17^\circ$. Conveniently, the semiconductor segment length $l_{\text{SEG}}$ depends not only on the angles $\theta_1$ and $\theta_2$, but also the separation S between bridge and NW. Increasing S from 9 $\mu$m to 17 $\mu$m reduced $l_{\text{SEG}}$ from $\sim 400$ nm to $\sim 40$ nm.

An important feature of our shadow epitaxy platform is the straightforward generalisation to full-shell geometries, achieved by radially copying the bridge design and depositing the coating from corresponding angles around the NW. **Figure 5d** shows an example full-shell JJ and the other geometries from Figure 1 can be implemented following the same strategy. Deposition of different materials from the various directions further in-
increases the possible functionality. Shadow epitaxy also applies to planar structures such as selective area grown nanostructures or vapour-liquid-solid NWs grown parallel to the substrate (Supplementary Section 9). Finally, we discuss the potential for large scale fabrication using vertical device structures in Supplementary Section 10.

CONCLUSION

In-situ-grown superconductor/semiconductor hybrid devices form the backbone of electronic implementations of quantum information ranging from topological qubits, gateable transmon devices and Andreev quantum dots. The shadow epitaxy platform transcends previous restrictions on the possible material combinations, and obviates the most potentially damaging fabrication steps, thus providing clear enhancement of device quality and functionality. Beyond these applications, electrical contact quality, reproducibility and surface disorder play an pivotal role in nearly all nanoscale devices, and thus improving material quality via shadow epitaxy holds the potential to strongly impact also conventional electronics, sensor-applications and optoelectronic devices.

EXPERIMENTAL SECTION

Fabrication of the shadow epitaxy platform. The platform is based on InAs (111)B-oriented substrates, capped with a 100 – 150 nm thick SiOx layer grown by plasma-enhanced chemical vapor deposition. The fabrication procedure is illustrated schematically in Supplementary Figure 1. The bridges were formed by two sequential wet etching steps using a single photolithographically defined mask (photoresist ZEP520A), with the custom pattern exposed using a Heidelberg μPG501 LED writer. Etching the SiOx using buffered hydrofluoric acid (6% in H₂O at room temperature) leaves strips of oxide in the desired bridge pattern, with typical length \( L \sim 10 \mu m \) and widths in the range \( W = 400 \text{ nm} - 2 \mu m \). The resist was removed and the InAs was subsequently etched using a 37:23:12 solution of C₆H₄O₇(40%):H₃PO₄(80%):H₂O₂ with the SiOx pattern acting as an etch mask. The anisotropic etch preferentially exposes (111)B InAs crystal planes and thereby forms trenches in the substrate, with a (111)B surface at the trench bottom suitable for NW growth. An etch time of 5 mins at room temperature produced trences with depth \( D \sim 7 \mu m \). The InAs etchant under-etches material from both sides of each SiOx strip and a void forms underneath the strips since their width \( W < D \). The result is SiOx bridges suspended above the etched InAs surface (Figure 1a). The process is highly reproducible and robust on a wafer scale (Supplementary Figure 2).

The potential to use the platform with antimide, nitride, silicon, and other NW materials is discussed in Supplementary Section 1. Electron beam lithography (PMMA A4.5 and EL13 resist stack) and e-beam deposition of Au were used to define the catalyst particles for NW growth. The platform is naturally compatible with multiple catalyst particles per bridge, and methods for randomly defining catalyst position. Note that fabricating the bridges requires merely a single photolithography step; the complex structures are obtained via relatively simple processing.

Nanowire hybrid growth. InAs NWs were grown via the Au catalyst-assisted vapour-liquid-solid mechanism in a solid-source Varian GEN-II MBE system following a two-step protocol. In the first step, NWs were grown vertically along the (111)B direction, using As₄ cracker temperature 500°C, substrate thermocouple temperature of 447°C and V/III flux ratio ≈ 10. A growth time of 80 mins resulted in 5 – 8 µm-long NWs. The second step involved growth at reduced substrate thermocouple temperature (350°C) and increased As cracker temperature (800°C) for 10 mins. These conditions promote radial overgrowth and flatter NW facets, optimal for subsequent superconductor deposition.

After InAs growth, the substrate was transferred under ultra-high vacuum to a metal evaporation chamber, with a freely rotatable sample holder that can be cooled to a thermocouple temperature of approx. –150°C using liquid nitrogen. The low temperature is used to decrease the size and pitch between the initial critical clusters, which promotes a continuous and flat film morphology. It also suppresses the potential for parasitic material to settle outside the shadow-mask defined regions, which may occur in particular for Al depositions at higher temperatures. The superconductor layers (Al, Ta, Nb, V) were deposited using e-beam evaporation at a fixed angle to align with the shadow mask design. The NWs grow with type-I, \{1100\} facets and the shadow mask design is oriented such that the superconductor deposition coats either 2 or 3 of the NW facets, as desired.

Electron microscopy. SEM characterisation of the substrates, as-grown NWs and finished devices was carried out in a JEOL 7800F using acceleration voltage \( V_{acc} = 5 – 10 \text{ kV} \). For TEM characterisation, NWs were transferred from the growth substrate to a carbon membrane grid using a micromanipulator under an optical microscope. TEM micrographs were obtained using either a Philips CM200 (Figure 2, center panels) with \( V_{acc} = 200 \text{ kV} \), a FEI Titan Analytical 80-300ST featuring a monochromator and \( V_{acc} = 300 \text{ kV} \) (Figure 2a, right panel) or a Philips 3000F with \( V_{acc} = 300 \text{ kV} \) (Figures. 2b,c, right panels). NWs were oriented with the beam parallel to an InAs facet (2110) zone-axis.

Device fabrication and measurement. NWs were transferred from the growth substrate to pre-patterned device substrates using a micromanipulator under an optical microscope. Ti/Au contacts and side gates were defined simultaneously using electron beam lithography and e-beam deposition. Ar⁺-ion milling was used immediately prior to contact deposition to remove native
InAs oxide and ensure ohmic contact to the NW. Electron transport measurements were conducted in an Oxford Triton dilution refrigerator with a base temperature \(\sim 20\) mK and a 6-1-T vector magnet. Standard low frequency (\(\sim 200\) Hz) lock-in techniques were used to measure differential conductance. For the island device in Figure 4, the cross-coupling of \(V_g\) to the tunnel barrier segments was compensated by sweeping \(V_{sg1,sg2}\) simultaneously with \(V_g\) using experimentally determined proportionality factors. Note the small offsets in Figures 4b,c. All electrical data throughout this work vanishes when measuring within a smaller gate range, as in Figures 4d-g. Raw electrical data and images for all figures are available from https://doi.org/10.17894/ucph.3a22ad5b-37fb-4495-b21d-42946e1e5fcc.

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**SUPPORTING INFORMATION**

Supporting Information is available at https://sid.erda.dk/share_redirect/BxJJoUWo0N

Raw electrical data and images for all figures are available from https://doi.org/10.17894/ucph.3a22ad5b-37fb-4495-b21d-42946e1e5fcc.